REMARKS

Claims 1-20 remain pending in the application.

35 U.S.C. § 102 Rejection:

Claims 1-5 were rejected under 35 U.S.C. § 102(b) as being anticipated by Clauberg, U.S. Patent 6,389,018. Applicant respectfully traverses this rejection.

The cited reference does not teach or suggest all of the elements of independent claim 1. The teachings of Clauberg were presented in the previous office action response.

Applicant's independent claim 1 recites, in pertinent part:

"A digital system that comprises: a plurality of units operating at a first clock rate, each unit configured to independently process a sequence of data items; and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate and configured to distribute **separate** sequences of data items through separate ports to the plurality of units" (emphasis added).

In the present office action, the Examiner maintains his position that Clauberg teaches a plurality of units operating at a first clock rate and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate and to distribute separate sequences of data items through separate ports to a plurality of units. Applicant respectfully disagrees with the Examiner's characterization of Clauberg.

Clauberg does not teach or suggest a domain crossover element configured to distribute separate sequences of data items through separate ports to the plurality of units. While Clauberg shows data items being processed in parallel within the parallel

processing unit, these items are regrouped and distributed therefrom in the same sequence at which they were received. In col. 5, lines 33-42, Clauberg states:

> "At the right hand side of the parallel processing paths 13.1-13.5, the sub-streams--after having been processed--are fed into a multiplexer 17 employed to provide an output stream 18 of fixed length cells on the slotted output medium 19. This multiplexer 17 is designed such that the original sequence of the cells, i.e. the chronological order on the input medium 11, **is re-established**. This means that not only the order of cells (like in a FIFO device; first in first out) but also the **exact arrangement** within the slots is maintained." (Emphasis added)

Thus, while individual data items may be processed separately in the parallel processing unit of Clauberg, they are received thereby and distributed therefrom **serially**, in the same, **original** sequence. In fact, even within the parallel processor, the data items are processed in the sequence at which they are originally received, as shown by Figs. 3A-3G, wherein cell A is the first received, the first fully processed, the first received by multiplexer 17, and first distributed on the slotted output medium 19, cell B is the second received, the second fully processed, the second received by multiplexer 17, the second distributed, and so forth. Since the sequence by which data cells are received, processed, and distributed in Clauberg is essentially unchanged, it is clear that the parallel processing unit of Clauberg does not distribute **separate** sequences at a second clock rate as recited in independent claim 1.

In the 'Response to Arguments' section of the present office action, the Examiner contends that Clauberg describes the use of a set of parallel processing means which slows down the processing time when each set of processing elements within a processing path is considered as a whole (i.e. the total time it takes to process a demultiplexed cell has been slowed down). Applicant respectfully disagrees with the Examiner's characterization, and submits that the processing time **is not slowed down**, but is merely **divided** among several parallel processing paths. Furthermore, the processing time of an individual demultiplexed cell is **not slowed down**, contrary to the

Examiner's assertion. Each cell shown in the examples given in Figs. 3A-3G advances by one position for each T, i.e. by one position for each slot duration. For example, cell A in Figs. 3A-3E advances to the demultiplexer (at time **T**) to processing unit 14.1 (at time **2T**) to processing unit 15.1 (at time **3T**) to the multiplexer (at time **4T**) to the slotted output medium (at time **5T**), or in other words, advances one position for each **T**. The fact that other cells may enter the parallel processing unit and may begin processing therein during the time cell A is progressing through the parallel processing unit does not change the fact that the rate (and thus the clock rate) at which cell A (and other subsequently received cells) progresses through the parallel processing unit is unchanged before its entry thereto, or during its processing therein. Furthermore, the fact that some processing units may have idle cycles where they are not processing a cell does not change the fact that they are still operating at the **same *clock*** rate, at which cells are received by or conveyed from the parallel processing unit.

Thus, despite the Examiner's assertions, Clauberg does not teach or suggest a plurality of units operating at a first clock rate or a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate. As is well known in the art, a clock rate is a frequency at which a clock operates, i.e. at which the clock transitions through a full cycle. The inverse of a clock's rate or frequency is its period. Clauberg teaches only a single duration, T, for cells entering, progressing through, and leaving the parallel processing unit, and thus only teaches a single clock rate, regardless of whether one or more clock cycles occur within the slot duration. In fact, Fig. 2 of Clauberg shows a slot duration of T. In col. 3, lines 44-46, Clauberg states:

> "The slotted character of the transmission medium is indicated by dividing up the time axis into slots. The slot duration is denoted by the letter `T`." (Emphasis added).

This is the only teaching or suggestion of a slot duration by Clauberg, which makes no distinction between the slot duration for cells entering the parallel processing unit,

progressing through parallel processing unit, or leaving the parallel processing unit. In contrast, Applicant's independent claim 1 recites a plurality of units operating at a **first** clock rate and a domain crossover element configured to receive a stream of data items at a **second** clock rate **different** from the first clock rate. These limitations are supported in Applicant's specification in Figs. 4 and 5 and the descriptions related thereto. More particularly, Fig. 4 illustrates a plurality of units which operate at a first clock rate (the rate of the *clock in* signal) and a domain crossover element configured to receive a stream of data items at a second clock rate (the rate of the *clock out* signal). Fig. 5 illustrates a first clock signal operating at a first clock rate (test.queue0.XCLK) and a second clock signal operating at a second clock rate (test.queue0.YCLK), wherein the second clock rate in this example is one half the first clock rate.

Essentially, Clauberg teaches a structure similar to a FIFO buffer, with some processing occurring in parallel in a parallel processing unit. However, the slot duration T, and therefore the clock **rate** at which data items are processed is the **same** slot duration (and thus clock rate) at which data items enter, progress through, and leave (in a single data stream) the parallel processing unit. This clock rate is **not** changed by the fact that data items may be processed in parallel nor is the clock rate changed by the fact that individual processing units within the parallel processing unit may experience idle cycles in which they are not processing any data item. Accordingly, Applicant submits that Clauberg does not teach or suggest a plurality of units operating at a **first** clock rate, and a **domain crossover element** configured to receive a stream of data items at a **second** clock rate different from the first clock rate as recited in independent claim 1.

For at least these reasons, Applicant submits that a case of anticipation has not been established, and thus respectfully requests removal of the 35 U.S.C. § 102(b) rejection.

35 U.S.C. § 103 Rejections:

Claims 6-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Chung, U.S. Patent 5,764,895. Claim 10 was rejected under 35

U.S.C. § 103(a) as being unpatentable over Clauberg in view of 5-Stage Johnson Counter, Talarek, U.S. Patent 6,628,679, and Segal, U.S. Patent 4,685,101. Claims 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Talarek and Segal. Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Clauberg in view of Talarek, Segal, and in further view of Karquist, U.S. Patent Application Publication 2003/0063626. Applicant respectfully traverses these rejections.

The proposed combination with Segal would change the principle of operation of Clauberg, and thus there is no suggestion to combine the references. Furthermore, Clauberg teaches away from claim 17. Independent claim 17 recites, in pertinent part:

> "sequentially selecting one of a plurality of registers at the first clock rate ... sequentially selecting one of a first subset of the plurality of registers at the second clock rate; sequentially selecting one of a second subset of the plurality of registers at the second clock rate, wherein the second subset is distinct from the first subset; and **concurrently** reading data items from the selected ones of the first and second subsets at the second clock rate"

In the office action, the Examiner states:

> "Clauberg and Talarek combined lack what [the] Segal describes: ... concurrently reading data items from the selected ones of the first and second subsets [at the second clock rate]" (emphasis added).

Thus, the Examiner acknowledges that neither Clauberg, Talarek, nor the combination thereof teach or suggest "concurrently reading data items from the selected ones of the first and second subsets" as recited in claim 17. Applicant submits that combining Segal with Clauberg (with or without Talarek) would change its principle of operation. In col. 5, lines 33-42, Clauberg states:

"At the right hand side of the parallel processing paths 13.1-13.5, the sub-streams--after having been processed--are fed into a multiplexer 17 employed to provide an output stream 18 of fixed length cells on the slotted output medium 19. This multiplexer 17 is designed such that the **original sequence** of the cells, i.e. the **chronological order** on the input medium 11, is re-established. This means that not only the order of cells (**like in a FIFO device**; first in first out) but also the **exact arrangement** within the slots is maintained." (Emphasis added)

In accordance with the citation above, as well as Figs. 1 and 3A-3G, it is clear that Clauberg teaches receiving and distributing cells to and from the parallel processing unit serially, wherein the cells are distributed in the same order in which they were received. In fact, cells are received by the multiplexer 17 (one slot duration **T** prior to distribution on the slotted output medium 19; see Clauberg, Fig. 1) in the same order in which they were originally received by the demultiplexer, and only one cell is received by the demultiplexer during any given slot duration. Thus, combining Segal with Clauberg (with or without Talarek) would change the principle of operation of re-establishing the **chronological order** of the cells and distributing them in the **exact arrangement** within the **slots** as they were first received. Applicant submits that the chronological order of cells could not be re-established, nor could cells be distributed in their exact arrangement within the slots if they were to be **concurrently** read from selected ones of the first and second subsets, as similarly recited in claim 17.

MPEP 2141.02(VI.) states that the prior art must be considered in its entirety, including disclosures that teach away from the claims. Applicant submits that Clauberg's teaching of re-establishing the chronological order of cells (as received on the input medium) like in a FIFO device, and their exact arrangement within the slots for distribution on the slotted output medium teaches away from Applicant's recited limitation of **concurrently** reading data items from the selected ones of the first and second subsets at the second clock rate. **MPEP 2143.01(VI.) states that the proposed modification cannot change the principle of operation of a reference.** Applicant

submits the Examiner's proposed combination of Segal with Clauberg such that data items are concurrently read from a first and a second subset of a plurality of registers would change Clauberg's principle of re-establishing the chronological order of cells (as received on the input medium) like in a FIFO device, and their exact arrangement within the slots for distribution on the slotted output medium. Thus, since Clauberg teaches away from claim 17, while the proposed combination with Segal changes Clauberg's principle of operation, **there is no suggestion to combine the references.**

In addition, since Clauberg teaches re-establishing the chronological order of cells (as received on the input medium) like in a FIFO device, and their **exact** arrangement within the slots for distribution on the slotted output medium, wherein the slots have a duration of T, Clauberg thus teaches away from sequentially selecting one of a plurality of registers at the first clock rate, selecting one of a first subset of the plurality of registers at the second clock rate, sequentially selecting one of a second subset of the plurality of registers at the second clock, and concurrently reading data items from the selected ones of the first and second subsets at the second clock rate as recited in claim 17.

For at least these reasons, Applicant submits a case of obviousness has not been established with respect to claim 17 or claims 18-20 which depend thereupon.

With respect to claims 6-10, **Clauberg teaches way from any combination that would include a domain crossover element configured to distribute separate sequences of data items through separate ports to the plurality of units**. As noted above in regard to the § 102(b) rejection, Clauberg teaches a system wherein cells are received, processed, and distributed in the **same** sequence. As such, Clauberg teaches away from a combination of features, such as that recited in independent claim 1, wherein the domain crossover element is configured to distribute separate sequences of data. As previously noted, **MPEP 2141.02(VI.) states that the prior art must be considered in its entirety, including disclosures that teach away from the claims.**

With respect to claims 6-9, the cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. Claims 6-9 depend from claim 1. For at least the reasons stated above with regard to the 35 U.S.C. § 102(b) rejection, Applicant submits that the cited references, taken singly or in combination, do not teach all of the elements of independent claim 1, and more particularly, do not teach or suggest a plurality of units operating at a first clock rate, and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate as recited in independent claim 1. Clauberg does not teach or suggest this combination of features, and Chung provides no teaching or suggesting that, when combined with Clauberg, would result in the claimed combination of features.

Furthermore, with respect to claims 6-9 as well as 10, **Clauberg teaches away from any combination that would include a plurality of units operating at a first clock rate, and a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate**. Since Clauberg teaches re-establishing the chronological order of cells (as received on the input medium) like in a FIFO device, and their **exact** arrangement within the slots for distribution on the slotted output medium, wherein the slots have a duration of **T**, Clauberg thus **teaches away** from a plurality of units operating at a **first clock rate**, and a domain crossover element configured to receive a stream of data items at a **second clock rate** different from the first clock rate. Accordingly, Clauberg teaches away from the combinations of references proposed by the Examiner in the rejections of claims 6-10.

For at least the reasons stated above, Applicant submits that a case of obviousness has not been established with regard to the various § 103(a) rejections. Accordingly, removal of these rejections is respectfully requested.

Allowed Claims:

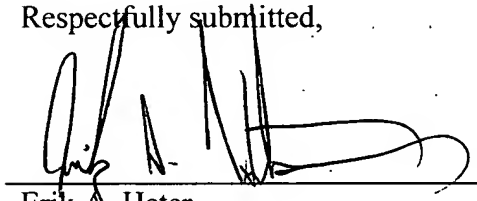
Claims 11-16 were allowed. Applicant appreciates Examiner's consideration of these claims.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-74100/BNK.

Respectfully submitted,



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